IN THE CLAIMS:

Please amend the claims as follows:

1. (Previously Presented) A circuit arrangement for compensating for disturbances in a signal generated by means of discrete multitone modulation (DMT), the signal generated by means of discrete multitone modulation exhibiting in the frequency domain a multiplicity of carrier frequencies which are used for transmitting data via a transmission channel, and each carrier frequency exhibiting a signal vector, comprising:

   (a) a multiplicity of first adder circuits, the multiplicity of first adder circuits being supplied with a first error signal vector and the multiplicity of first adder circuits adding the first error signal vector to at least one first signal vector in order to generate an error-corrected first signal vector; and

   (b) a multiplicity of first multiplier circuits which precede the multiplicity of first adder circuits and multiply the first error signal vector by adjustable coefficients, wherein the first error signal vector is a signal vector of a carrier frequency which is not used for transmitting data via the transmission channel.

2. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the first error signal vector is a signal vector of a carrier frequency

which, in the frequency domain, is adjacent to a carrier frequency which is used for transmitting data via the transmission channel.

3. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the first error signal vector is a signal vector of a carrier frequency which, in the frequency domain, immediately precedes a carrier frequency which is used for transmitting data via the transmission channel.

4. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the circuit arrangement also exhibits the following features:

(a) at least one further multiplicity of first adder circuits which follow the multiplicity of first adder circuits, the at least one further multiplicity of first adder circuits in each case being supplied with a further error signal vector and the at least one further multiplicity of first adder circuits adding the respective further error signal vector to the at least one signal vector in order to generate a progressively error-corrected signal vector; and

(b) at least one further multiplicity of first multiplier circuits which precede the at least one further multiplicity of first adder circuits and multiply the respective further error signal vector by adjustable coefficients.

5. (Previously Presented) The circuit arrangement as claimed in claim 4, wherein the respective further error signal vector is in each case a signal

vector of a carrier frequency which is not used for transmitting data via the transmission channel.

6. (Previously Presented) The circuit arrangement as claimed in claim 4, wherein the respective further error signal vector is in each case a previous version of a particular error signal vector.

7. (Previously Presented) The circuit arrangement as claimed in claim 6, wherein the circuit arrangement has at least one buffer circuit for storing a previous version of an error signal vector.

8. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the circuit arrangement also exhibits the following features:

(a) a decision circuit which maps the error-corrected first signal vector into a value-discrete first signal vector; and

(b) a subtracting circuit for forming a second error signal vector which subtracts the first signal vector (a1', b1') and the value-discrete first signal vector from one another, the second error signal vector being used for generating an error-corrected second signal vector of a second signal vector of a carrier frequency which is immediately adjacent to the carrier frequency of the first signal vector.

9. (Previously Presented) The circuit arrangement as claimed in claim 8, wherein the circuit arrangement also exhibits the following features:

(a) a multiplicity of second adder circuits, the multiplicity of second adder circuits being supplied with the second error signal vector and the multiplicity of second adder circuits (12 1, 13 1) adding the second error signal vector to the second signal vector in order to generate the error-corrected second signal vector; and

(b) a multiplicity of second multiplier circuits which precede the multiplicity of second adder circuits and multiply the second error signal vector by adjustable coefficients.

10. (Previously Presented) The circuit arrangement as claimed in claim 9, wherein the circuit arrangement also exhibits the following features:

(a) a further decision circuit which maps the error-corrected second signal vector into a value-discrete second signal vector; and

(b) a further subtracting circuit for forming a third error signal vector which subtracts the second signal vector and the value-discrete second signal vector from one another, the third error signal vector being used for generating an error-corrected third signal vector of a third signal vector of a carrier frequency which is immediately adjacent to the carrier frequency of the second signal vector.

11. (Currently Amended) A circuit arrangement for compensating for disturbances in a signal generated by means of discrete multitone modulation (DMT), the signal generated by means of discrete multitone modulation

exhibiting in the frequency domain a multiplicity of carrier frequencies which are used for transmitting data via a transmission channel, and each carrier frequency exhibiting a signal vector, comprising:

(a) decision circuits which are in each case supplied with a reference signal vector and which map the respective reference signal vector into a respective value-discrete reference signal vector;

(b) subtracting circuits for forming a respective error signal vector which subtract the respective reference signal vector and the respective value-discrete reference signal vector from one another;

(c) more than one group[[s]] of first adder circuits, each group of first adder circuits in each case being supplied with an error signal vector and the groups of first adder circuits adding the respective error signal vectors to each of at least one signal vector in order to generate a progressively error-corrected signal vector; and

(d) groups of first multiplier circuits which in each case precede a group of first adder circuits and multiply the respective error signal vector by adjustable coefficients.

12. (Previously Presented) The circuit arrangement as claimed in claim 1, wherein the adjustable coefficients can be adjusted by means of a correcting variable.

13. (Original) The circuit arrangement as claimed in claim 12, wherein a power of 2 is selected for the correcting variable.

14. (Previously Presented) A method for compensating for disturbances in a signal generated by means of discrete multitone modulation (DMT), the signal generated by means of discrete multitone modulation exhibiting in the frequency domain a multiplicity of carrier frequencies which are used for transmitting data via a transmission channel, and each carrier frequency exhibiting a signal vector, comprising the following steps:

(a) multiplying at least one error signal vector by adjustable coefficients; and

(b) adding the at least one error signal vector multiplied by the adjustable coefficients to at least one signal vector in order to generate an error-corrected signal vector, wherein the at least one error signal vector is a signal vector of a carrier frequency which is not used for transmitting data via the transmission channel.

15. (Previously Presented) The method as claimed in claim 14, wherein the first error signal vector is a signal vector of a carrier frequency which, in the frequency domain, is adjacent to a carrier frequency which is used for transmitting data via the transmission channel.

16. (Previously Presented) The method as claimed in claim 14, wherein the first error signal vector is a signal vector of a carrier frequency which, in the frequency domain, immediately precedes a carrier frequency which is used for transmitting data via the transmission channel.

17. (Previously Presented) The method as claimed in claim 14, wherein the method also exhibits the following steps:

(a) multiplying a respective further error signal vector by adjustable coefficients; and

(b) adding the respective further error signal vector multiplied by the adjustable coefficients to the at least one signal vector in order to generate a progressively error-corrected signal vector.

18. (Previously Presented) The method as claimed in claim 17, wherein the respective further error signal vector is in each case a signal vector of a carrier frequency which is not used for transmitting data via the transmission channel.

19. (Previously Presented) The method as claimed in claim 17, wherein the respective further error signal vector is in each case a previous version of a particular error signal vector.

20. (Previously Presented) The method as claimed in claim 14, wherein the method also exhibits the following steps:

(a) mapping the error-corrected first signal vector into a value-discrete first signal vector; and

(b) subtracting the first signal vector and the value-discrete first signal vector from one another in order to form a second error signal vector, the second error signal vector being used for generating an error-corrected second signal vector of a second signal vector of a carrier frequency which is immediately adjacent to the carrier frequency of the first signal vector.

21. (Previously Presented) The method as claimed in claim 20, wherein the method also exhibits the following steps:

(a) multiplying the second error signal vector by adjustable coefficients; and

(b) adding the second error signal vector multiplied by the adjustable coefficients to the second signal vector in order to generate the error-corrected second signal vector.

22. (Previously Presented) The method as claimed in claim 21, wherein the method also exhibits the following steps:

(a) mapping the error-corrected second signal vector into a value-discrete second signal vector; and

(b) subtracting the second signal vector and the value-discrete second signal vector from one another in order to form a third error signal

vector, the third error signal vector being used for generating an error-corrected third signal vector of a third signal vector of a carrier frequency which is immediately adjacent to the carrier frequency of the second signal vector.

23. (Currently Amended) A method for compensating for disturbances in a signal generated by means of discrete multitone modulation (DMT), the signal generated by means of discrete multitone modulation exhibiting in the frequency domain a multiplicity of carrier frequencies which are used for transmitting data via a transmission channel, and each carrier frequency exhibiting a signal vector, comprising the following steps:

(a) mapping a plurality of respective reference signal vectors into a plurality of respective value-discrete reference signal vectors;

(b) subtracting the plurality of respective reference signal vectors and the plurality of respective value-discrete reference signal vectors from one another in order to form a plurality of respective error signal vectors;

(c) multiplying each of the plurality of respective error signal vectors by adjustable coefficients; and

(d) adding the plurality of respective error signal vectors multiplied by the adjustable coefficients to each of at least one signal vector in order to generate a progressively error-corrected signal vector.

24. (Previously Presented) The method as claimed in claim 14, wherein the adjustable coefficients can be adjusted by means of a correcting variable.

25. (Original) The method as claimed in claim 24, wherein a power of 2 is selected for the correcting variable.

26. (New) A circuit arrangement for compensating for disturbances in a signal generated by means of discrete multitone modulation (DMT), the signal generated by means of discrete multitone modulation exhibiting in the frequency domain a multiplicity of carrier frequencies which are used for transmitting data via a transmission channel, and each carrier frequency exhibiting a signal vector, comprising:

(a) decision circuits which are in each case supplied with a reference signal vector and which map the respective reference signal vector into a respective value-discrete reference signal vector;

(b) subtracting circuits for forming a respective error signal vector which subtract the respective reference signal vector and the respective value-discrete reference signal vector from one another;

(c) a multiplicity of first adder circuits, the multiplicity of first adder circuits in each case being supplied with an error signal vector from an adjacent carrier frequency and the multiplicity of first adder circuits adding the respective adjacent error signal vector to at least one signal vector in order to generate an error-corrected signal vector; and

(d) a multiplicity of first multiplier circuits which in each case precede the multiplicity of first adder circuits and multiply the respective adjacent error signal vector by adjustable coefficients.